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| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/606,525 | PETERSON, KENNETH A. | |
| | Examiner | Art Unit | |
| | Shouxiang Hu | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/22/04*.

2. ☒ The allowed claim(s) is/are *6-9,12-20,22 and 48*.

3. ☒ The drawings filed on *26 June 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

**Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20050411* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Shouxiang Hu

**SHOUXIANG HU**
**PRIMARY EXAMINER**

## EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Robert D. Walton (RN: 45,604) on April 11, 2005.

The application has been amended as follows:

IN THE CLAIMS

1-5. (CANCELLED)

6. (CURRENTLY AMENDED) A microelectronic device, comprising:

an electrically insulating substrate;

a first electrical conductor disposed on the substrate;

a microelectronic device attached to the substrate, wherein the device comprises an active area and a passive area;

a second electrical conductor disposed on the device, located within the passive area;

an electrical interconnection formed between the first and second electrical conductors; and

an electrically insulating, protective coating covering the first and second electrical conductors, the electrical interconnection, and the passive area, ~~but not covering the~~

~~active area~~ a portion of the protective coating being removed so as to expose the active area before MEMS elements in the active area being released,

wherein the thickness of the protective coating is less than or equal to 100 microns.

7. (Original) The microelectronic device of claim 6, wherein the substrate comprises one or more electrically insulating materials selected from the group consisting of ceramic, plastic, printed wiring board material, polymer, multi-layered material, LTCC ceramic multilayered material, and HTCC ceramic multilayered material.

8. (PREVIOUSLY PRESENTED) The microelectronic device of claim 6, wherein the substrate comprises a package having a geometry selected from the group consisting of DIP, ceramic dual inline packaging (or, CERDIP), quad flatpack, pin grid array, leadless chip carrier, and a leaded flatpack.

9. (CURRENTLY AMENDED) The microelectronic device of claim 6, comprising one or more active elements, disposed within the active area, selected from the group consisting of ~~MEMS elements,~~ optically sensitive elements, temperature sensitive elements, heat sensitive elements, chemical sensitive elements, pressure sensitive elements, and microsensors.

10. (CANCELLED)

11. (CANCELLED)

12. (Original) The microelectronic device of claim 6, wherein the electrical interconnection comprises a wirebond or a flip-chip ball or bump.

13. (PREVIOUSLY PRESENTED) The microelectronic device of claim 6, wherein the device is flip-chip mounted to the substrate, and wherein the substrate comprises an

aperture aligned over the active area, whereby the active area is accessible through the aperture.

14. (CURRENTLY AMENDED) The microelectronic device of claim [[6]] 13, wherein the package comprises a transparent window disposed across the aperture.

15. (Original) The microelectronic device of claim 6, wherein the electrically insulating protective coating comprises one or more materials selected from the group consisting of a vapor-deposited coating, a vacuum vapor deposited coating, a chemical vapor deposited coating, a water-insoluble coating, a water-soluble coating, a dry-etchable coating, a conformal coating, a pin-hole free coating, parylene, a photopatternable/photoimagable material, photoresist, a low viscosity photoresist, an epoxy based negative resist, SU-8, SU-8 2000, a sputtered coating, an evaporated coating, a ceramic coating, silicon nitride, aluminum oxide, mullite, a sprayed coating, a self-assembled monolayered material, cyanoacrylate, perfluoropolyether, hexamethyidisilazane, perfluorodecanoic carboxylic acid, silicon dioxide, TEOS, silicate glass, a fast-etch glass, silicon, and polysilicon.

16. (Original) The microelectronic device of claim 6, wherein the electrically insulating protective coating comprises one or more materials selected from the group consisting of poly-para-xylylene, poly-para-xylylene that has been modified by the substitution of a chlorine atom for one of the aromatic hydrogens, and poly-para-xylylene that has been modified by the substitution of the chlorine atom for two of the aromatic hydrogens.

17. (PREVIOUSLY PRESENTED) The microelectronic device of claim 6, wherein the passive area comprises an integrated circuit.

18. (PREVIOUSLY PRESENTED) The microelectronic device of claim 6, further comprising an electrically conductive overcoat deposited on top of the electrically

insulating protective coating, whereby the electrically conductive overcoat provides electromagnetic shielding.

19. (PREVIOUSLY PRESENTED) The microelectronic device of claim 18, wherein the electrically conductive overcoat comprises one or more conductive materials selected from the group consisting of a metal, gold, tungsten, nickel, aluminum, copper, titanium, molybdenum, tin, tantalum, a metal alloy, an electrically-conductive polymer, carbon, doped carbon, and doped silicon.

20. (PREVIOUSLY PRESENTED) The microelectronic device of claim 6, wherein the conductive overcoat is continuous across two or more adjacent electrical interconnections.

21. (CANCELLED)

22. (PREVIOUSLY PRESENTED) The microelectronic device of claim 6, wherein the substrate comprises an interposer or an interposer with an aperture aligned with the active area.

23-47. (CANCELLED)

48. (PREVIOUSLY PRESENTED) The microelectronic device of claim 6, wherein the thickness of the protective coating is less than or equal to 100 angstroms.

***Allowable Subject Matter***

Claims 6-9, 12-20, 22 and 48 are allowed.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
April 11, 2005

SHOUXIANG HU
PRIMARY EXAMINER